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# Limiting Amplifier for Applications up to 2.1 Gbps

# M02040

## M02040 can support either a 3.3V or 3.3V/5V supply

The M02040 is an integrated high-gain limiting amplifier. Featuring PECL outputs, the M02040 is usable in applications up to 2.1 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02040 operates with a 3.3V or 3.3V/5V supply.

The M02040 also includes two analog RSSI outputs proportional to either the average or peak-to-peak input signal and a programmable signal-level detector allowing the user to set thresholds at which the logic outputs are enabled. The M02040 is pin compatible with the M02050 2.5 Gbs post amplifier.

### Inputs

The data inputs are internally connected to $V_{TT}$ via 50Ω resistors, and generally need to be AC coupled. The nominal $V_{TT}$ voltage is 2.85V because of the internal resistor divider to $V_{CC}$ which means this is the DC potential on the data inputs. See the applications information section for further details on choosing the AC-coupling capacitor.

### DC Offset Compensation

M02040 contains an internal DC autozero circuit that can remove the effect of DC offsets without using external components. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically 25 kHz.

## KEY FEATURES

- 4 mV maximum input sensitivity at 2.1 Gbps
- PECL outputs
- Average and peak-to-peak receive power monitor outputs
- Jam function
- Low power (< 180 mW)
- 16 pin 3x3 QFN, standard/green package

### PECL Outputs

The M02040 features 100k/300k PECL compliant outputs. The outputs may be terminated using any standard AC or DC-coupling PECL termination technique. AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drive and compatibility with non-PECL interfaces.

### Loss of Signal (LOS)

The M02040 features input signal level detection over an extended range. Using an external resistor, $R_{ST}$, between pin $ST_{SET}$ and $V_{CC}$, the user can program the input signal threshold. The LOS signal is active when the signal is below the threshold value. The signal detection circuitry has the equivalent of 3.5 dB (typical) electrical hysteresis. $R_{ST}$ establishes a threshold voltage at the $ST_{SET}$ pin. Internally, the input signal level is monitored by the level detector (which also outputs the $RSSI_{PP}$ voltage). As described in the $RSSI_{PP}$ section, this voltage is proportional to the input signal peak-to-peak value. The voltage at $ST_{SET}$ is internally

compared to the signal level from the level detector. When the level detector voltage is less than $V(ST_{SET})$, LOS is asserted and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis above $V(ST_{SET})$, LOS is de-asserted.

### Peak-to-Peak Received Strength Indicator ($RSSI_{PP}$)

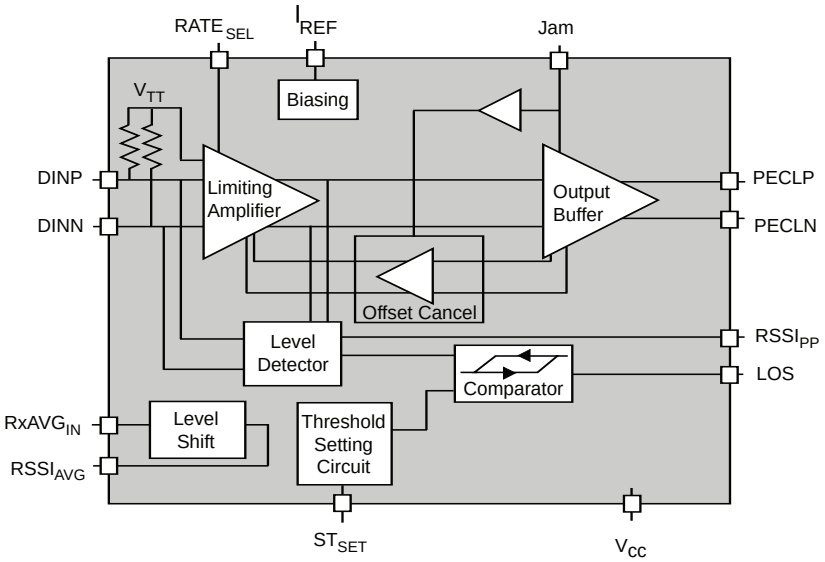
The $RSSI_{PP}$ output voltage is logarithmically proportional to the peak to peak level of the input signal. It is not necessary to connect an external capacitor to this output. Internally, the RSSI voltage is compared with a user selectable reference to determine loss of signal as described in the previous section.

### Jam Function

When asserted, the active high power down (Jam) pin forces the outputs to a logic "one" state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It, therefore, inhibits the data outputs toggling due to noise when there is no signal present ("squelch"). In order to implement this function, LOS should be connected to the Jam pin, thus forcing the data outputs to a logic "one" state when the signal falls below the threshold.

### Averaged Received Strength Indicator ($RSSI_{AVG}$)

The $RSSI_{AVG}$ output current is a mirrored version of the $RxAVG_{IN}$ current from compatible TIAs. It sources rather than sinks the current making it compatible with DDMI type interfaces.




M02040 Block Diagram

## Product Highlights

### Applications

- 1.06, 2.12 Gbps Fibre Channel
- 1.25 Gbps Ethernet

### Features

- Operates with a 3.3V ("-14") or 3.3V/5V ("-15") supply
- 4 mV maximum input sensitivity at 1.25 Gbps
- PECL outputs
- Peak-to-peak and average receive power monitor outputs

### Ordering Information

- M02040-14: 3.3V
- M02040-15: 3.3/5V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